CLAIMS

What is claimed is:

1. A method comprising:

forming a plurality of active regions on a substrate;

depositing an insulating layer over the active regions;

removing a portion of the insulating layer to form a one-dimensional slot and to provide access to the active regions; and

forming a bit line in the slot in contact with the active regions.

2. The method of claim 1, wherein the active regions comprise source and drain (S/D) regions.

3. The method of claim 1, wherein removing further comprises:

depositing a resist layer over the insulating layer;

patterning and exposing the resist using a one-dimensional mask, and removing developed portions of the resist; and

etching the insulating layer.

4. The method of claim 3, wherein patterning the resist comprises using an off-axis illumination scheme.

5. The method of claim 1, wherein the insulating layer is an interlayer dielectric (ILD).

6. The method of claim 5, wherein the ILD is silicon dioxide (SiO_2).

7. The method of claim 1, further comprising:

forming a plurality of gate stacks on the substrate coupled to the active regions;

wherein depositing an insulating layer comprises depositing an insulating layer over the gate stacks; and

wherein removing a portion of the insulating layer comprises exposed the gate stacks.

8. The method of claim 7, wherein forming a plurality of gate stacks includes forming spacers adjacent to the gate stacks.

9. The method of claim 8, wherein the spacers are nitride spacers.

10. The method of claim 1, wherein forming a bit line comprises depositing a conductive material in the slot, and polishing the conductive material.

11. The method of claim 1, wherein a width of the slot is insignificant compared to a length of the slot.

12. A flash memory cell comprising:

a plurality of gate stacks formed on a substrate, and a plurality of active regions formed in the substrate;

an interlayer dielectric (ILD) deposited over the gate stacks and the active regions;

a one-dimensional slot patterned in the ILD to provide access to the active regions; and

a bit line formed in the slot to contact the active regions.

13. The flash memory cell of claim 12, wherein the bit line comprises a tungsten plug.

14. The flash memory cell of claim 12, wherein the flash memory cell is a NOR memory cell.

15. The flash memory cell of claim 12, further comprising:

a plurality of nitride spacers adjacent to the gate stacks.

16. The flash memory cell of claim 12, wherein the gate stacks comprise a control gate and a floating gate.

17. The flash memory cell of claim 16, further comprising a word line to control the control gate.

18. A method comprising:

providing a silicon substrate;

forming a plurality of gate stacks on the substrate;

implanting source and drain (S/D) extensions in the substrate;

forming nitride spacers adjacent to the gate stacks;

implanting a plurality of S/D regions in the substrate;

depositing an interlayer dielectric (ILD) over the substrate;

removing a portion of the ILD to form a one-dimensional slot and expose the gate stacks; and

depositing a conductive material in the slot to contact the S/D regions and form a bit line.

19. The method of claim 18, wherein removing a portion of the ILD further comprises:

depositing a resist layer over the ILD;

exposing the resist layer to an ultraviolet (UV) light through a mask;

removing an exposed portion of the resist; and

etching the ILD.

20. The method of claim 19, wherein exposing the resist layer comprises using an off-axis printing scheme.

21. The method of claim 20, wherein the off-axis printing scheme includes using a dipole light source.

22. The method of claim 18, wherein depositing a conductive material in the slot further comprises:

depositing a tungsten plug in the slot; and

polishing the tungsten plug.